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10/609,264	06/26/2003	Nicholas G. Samra	42P16354	8108

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Lester J. Vincent
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025

EXAMINER	
JOHNSON, BRIAN P	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/609,264	SAMRA ET AL.	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are pending.

Papers Filed

2. Examiner acknowledges receipt of amendments and remarks filed on 14 May 2007.

Title

3. The title is accepted. Objection is withdrawn.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 23-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Levy et al. (U.S. Patent No. 6,092,175) hereinafter referred to as Levy.

6. As per claim 23, Levy discloses a method comprising:

initializing a register allocation table (RAT) to map a first group of logical registers to a second group of physical registers; *Fig. 15 is evidence of such a mapping.*

dividing a freelist of registers in half if a processor associated with the free list is in multi-thread (MT) mode; *Levy's embodiment 1 discloses segregating rename register by thread.*

undividing the freelist of registers if the processor is in single-thread (ST) mode. *Levy's 2nd embodiment discloses an undivided rename register region. If the processor is in ST mode, the single thread has access to all of said rename registers.*

7. As per claim 24, Levy discloses the method of claim 23 further comprising transitioning from ST mode to MT mode, the second group of physical registers being interspersed throughout a physical register file. *Figure 15 is an example disclosing physical registers spread throughout the register file with multiple threads running. The registers associated with the first thread are spread throughout the register file.*

8. As per claim 25, Levy discloses the method of claim 24 wherein the second group of physical registers remain interspersed throughout the physical register file after the transition from ST to MT mode. *The register file in Figure 15 exemplifies the*

physical registers being spread out throughout the file, regardless of what thread they are associated with.

9. As per claim 26, Levy discloses the method of claim 23 further comprising transitioning from MT mode to ST mode, the second group of physical registers being interspersed throughout a physical register file. *The examiner asserts that in Figure 15, when the second thread terminates, the first thread's logical registers will still point to the same physical registers as "a register can only be freed when the hardware can guarantee that the register's value is 'dead'" (Col. 16 line 41-42)*

10. As per claim 27, Levy discloses the method of claim 26 wherein the second group of physical registers remain interspersed throughout the physical register file after the transition from MT to ST mode. *The examiner asserts that in Figure 15, when the second thread terminates, the first thread's logical registers will still point to the same physical registers as "a register can only be freed when the hardware can guarantee that the register's value is 'dead'" (Col. 16 line 41-42)*

11. As per claim 28, Levy discloses the method of 23 wherein the logical registers are allocated to the physical registers independently of the relative position of the logical registers to each other. *Figure 15 is evidence of physical registers being mapped to logical registers with no regard for physical location relative to each other.*

12. As per claim 29, Levy discloses the method of claim 28 wherein, in MT mode, the sum of the entries in the freelist and the number of logical registers associated with a single thread equals the number of physical registers within the physical register file. *The examiner asserts that when a single thread is running, Levy's 3rd embodiment ensures that all unused physical registers are accessible by said first thread. Therefore, the sum of the available threads (those in the free list) plus those in use by the first thread equal the total number of physical registers in the register file.*

As per claim 30, Levy discloses the method of claim 29 further comprising a indicating a first physical register in the freelist after an instruction associated with data stored in the first physical register is retired. (Col. 16 lines 39-44) *The examiner asserts that since a register's "contents may be overwritten" the register is added to freelist 70.*

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levy (U.S. Patent No. 6,092,175) in view of Leibholz (U.S. Patent No. 6,954,846).

13. As per claim 1, Levy discloses an apparatus comprising: a physical register file (Fig. 1 register file 37) in which data associated with instructions of a computer program are stored in an order that is independent of whether a processor executing the instructions is in a multithread (MT) mode or a single-thread (ST) mode. *The examiner asserts that the order in which data is stored in the register file is not dependant of how many threads are running, but rather which registers are available to the running threads. Fig. 15*

Levy fails to disclose that the physical registers are to be divided equally among a plurality of threads when operating in MT mode.

Leibholz discloses physical registers being divided equally amount a plurality of threads when operating in MT mode (col 1 lines 56-67 and col 4 lines 19-20)

Levy and Leibholz similarly support a flexible approach to register files (Leibholz col 1 lines 49-53 and Levy col 3 lines 17-48). Leibholz, however, utilizes a technique that solves a further problem of resource contention (col 1 lines 43-67). For this reason, Levy would be motivated to utilize the teachings of Leibholz.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Levy and allow the threads to utilize private register files in multi-threaded mode, as shown in Leibholz.

14. As per claim 2, Levy/Leibholz discloses the apparatus of claim 1 further comprising at least one register allocation table (RAT) (Fig. 4 register mapping table 72)

to indicate allocation of the data from logical registers to physical registers within the physical register file. (Col. 9 lines 27-32)

15. As per claim 3, Levy/Leibholz discloses the apparatus of claim 1 further comprising a list of physical registers (Fig. 4 free register list 70) within the physical register file that are not allocated to a logical register, (Col. 9 line 31-32) entries in the list being completely allocated to a first thread while the processor is in ST mode and entries in the list being partitioned such that a first portion of the entries are allocated to a first thread and a second portion of the entries are allocated to a second thread while the processor is in MT mode. *Levy's 2nd embodiment (described in Col. 10 lines 5-17 and pictured in Fig. 5B) fulfills the requirements of this claim. When only one thread is running, that thread has access to all of the renaming registers common to any running threads. When two threads are running, they share the common renaming registers and a partition can be made between registers associated with the first and second threads.*

16. As per claim 4, Levy/Leibholz discloses the apparatus of claim 3 wherein a first portion (Fig. 5B registers 86 in combination with the renaming registers) of all of the physical registers in the physical register file are allocated to the first thread and a second portion (Fig. 5B registers 88) of all of the physical registers in the physical register file are allocated to the second thread if the processor is in ST mode, the first portion of all of the physical registers being larger than the second portion of all of the

physical registers. *The examiner asserts that if the processor is in ST mode, only one thread is running. This thread, therefor, has exclusive access to the shared renaming registers. Since the 2nd embodiment discloses that each thread has reserved architectural registers, regardless of whether there is an active thread associated with said thread or not, each of the first and second thread has a portion of the physical register file reserved for it.*

17. As per claim 5, Levy/Leibholz discloses the apparatus of claim 4 wherein the second thread is dormant if the processor is in ST mode. *The examiner asserts that if the processor is in Single-thread mode, only one thread is running. Inherently, any second thread cannot be running, and must therefor be dormant.*

18. As per claim 6, Levy/Leibholz discloses the apparatus of claim 4 wherein the first portion of all of the physical registers within the physical register file remain allocated to the first thread after the processor transitions to MT mode until instructions associated with data within the first portion of all of the physical registers within the physical register file are retired. *The examiner asserts that the processor disclosed by Levy inherently does not reallocate a currently used physical register to a newly started thread until the instruction(s) associated with said register are retired. (Col. 16 lines 39-44)*

19. As per claim 7, Levy/Leibholz discloses the apparatus of claim 6 wherein the physical registers associated with the retired instructions are indicated within the list of

physical registers. (Col. 16 lines 39-44) *The examiner asserts that since a register's "contents may be overwritten" the register is added to freelist 70.*

20. As per claim 8, Levy/Leibholz discloses an apparatus comprising: first means (Fig. 4 free list 70) for storing data for use by a microprocessor, the first means being allocated equally among a plurality of threads during a second mode of operation of the microprocessor (see claim 1) and in an order that is independent of whether the microprocessor is in the second mode of operation or a first mode of operation, in which only a single thread is processed; second means for allocating the logical registers to the physical registers. (Fig. 4 register mapping table 72) for allocating the logical registers to the physical registers. *The examiner asserts that in Levy's 3rd embodiment, when two threads are running, architectural registers are partitioned by thread such that while some may not be used, they are reserved for a specific thread. When only one thread is running, all of the physical registers are available for that thread.*

21. As per claim 10, Levy/Leibholz discloses the apparatus of claim 8 wherein the second means comprises a register allocation table (Fig. 4 table 72) to indicate the allocation of the logical registers to the physical registers. (Col. 9 lines 27-32)

22. As per claim 11, Levy/Leibholz discloses the apparatus of claim 8 wherein the second means comprises a plurality of register allocation tables (Fig. 15 tables 120 and 122) to indicate the allocation of the logical registers to the physical registers, each of

the plurality of register allocation tables being associated with a separate thread of instructions.

23. As per claim 12, Levy/Leibholz discloses the apparatus of claim 11 wherein the first mode of operation is a single thread mode and the second mode is a multiple-thread mode.

24. As per claim 13, Levy/Leibholz discloses the apparatus of claim 12 wherein the first means is a register file comprising a list of the physical registers that are not allocated to the logical registers. (Fig. 4 free list 70 and Col. 9 line 31-32)

25. As per claim 14, Levy/Leibholz discloses the apparatus of claim 13 wherein, in the second mode of operation, the sum of the number of physical registers in the list and the number of logical registers associated with a single thread equals the number of physical registers within the physical register file. *The examiner asserts that when a single thread is running, Levy's 3rd embodiment ensures that all unused physical registers are accessible by said first thread. Therefore, the sum of the available threads (those in the free list) plus those in use by the first thread equal the total number of physical registers in the register file.*

26. As per claim 15, Levy/Leibholz discloses the apparatus of claim 14 wherein a first physical register is indicated in the list after an instruction associated with data stored in

the first physical register is retired. (Col. 16 lines 39-44) *The examiner asserts that since a register's "contents may be overwritten" the register is added to freelist 70.*

27. As per claim 16, Levy/Leibholz discloses a system comprising: a memory unit to store a first and second thread of instructions (Fig. 1 instruction cache 24); a processor to perform the first and second thread of instructions (Fig. 1), the processor comprising a physical register file (Fig. 1 register file 37) wherein data corresponding to the first and second thread of instructions are stored in an order independent of whether the processor is in a multithread (MT) mode or a single-thread (ST) mode, wherein the physical register file is to be allocated equally among a plurality of threads when operating in MT mode (see claim 1).

28. As per claim 17, Levy/Leibholz discloses the system of claim 16 wherein the processor further comprises at least one register allocation table (RAT) (Fig. 4 register mapping table 72) to indicate allocation of the data from logical registers to physical registers within the physical register file. (Col. 9 lines 27-32)

29. As per claim 18, Levy/Leibholz discloses the system of claim 16 further comprising a list of physical registers not allocated to a logical register (Fig. 4 free list 70), entries in the list being completely allocated to the first thread while the processor is in ST mode and entries in the list being partitioned such that a first portion of the entries are allocated to the first thread and a second portion of the entries are allocated to the

second thread while the processor is in MT mode. *Levy's 2nd embodiment (described in Col. 10 lines 5-17 and pictured in Fig. 5B) fulfills the requirements of this claim. When only one thread is running, that thread has access to all of the renaming registers common to any running threads. When two threads are running, they share the common renaming registers and a partition can be made between registers associated with the first and second threads.*

30. As per claim 19, Levy/Leibholz discloses the system of claim 18 wherein a first portion (Fig. 5B registers 86 in combination with the renaming registers) of all of the physical registers in the physical register file are allocated to the first thread and a second portion (Fig. 5B registers 88) of all of the physical registers in the physical register file are allocated to the second thread if the processor is in ST mode, the first portion of all of the physical registers being larger than the second portion of all of the physical registers. *The examiner asserts that if the processor is in ST mode, only one thread is running. This thread, therefor, has exclusive access to the shared renaming registers. Since the 2nd embodiment discloses that each thread has reserved architectural registers, regardless of whether there is an active thread associated with said thread or not, each of the first and second thread has a portion of the physical register file reserved for it.*

31. As per claim 20, Levy/Leibholz discloses the system of claim 19 wherein the second thread is dormant if the processor is in ST mode. *The examiner asserts that if*

the processor is in Single-thread mode, only one thread is running. Inherently, any second thread cannot be running, and must therefor be dormant.

32. As per claim 21, Levy/Leibholz discloses the system of claim 19 wherein the first portion of all of the physical registers within the physical register file remain allocated to the first thread after the processor transitions to MT mode until instructions associated with data within the first portion of all of the physical registers within the physical register file are retired. *The examiner asserts that the processor disclosed by Levy inherently does not reallocate a currently used physical register to a newly started thread until the instruction(s) associated with said register are retired. (Col. 16 lines 39-44)*

33. As per claim 22, Levy/Leibholz discloses the system of claim 21 wherein the physical registers associated with the retired instructions are indicated within the list of physical registers. (Col. 16 lines 39-44) *The examiner asserts that since a register's "contents may be overwritten" the register is added to freelist 70.*

Response to Arguments

3. Applicant's arguments filed 14 May 2007 have been fully considered but they are not all persuasive.

4. Applicant states:

"First, the Examiner asserted that Fig. 15 of Levy discloses the limitation of initializing a register allocation table (RAT) to map a first group of logical registers to a second group of physical registers. Applicants respectfully disagree. As Fig. 15 of Levy clearly shows, Fig. 15 a figure illustrating a mapping

relationship from references to architectural registers in instructions to renaming registers. Architectural registers in instructions are not logical registers. Also Fig. 15 does not show a register allocation table (RAT) but only illustrates architectural registers in instructions can be mapped to rename registers. Moreover, Fig. 15 does not show, expressly or inherently, initializing the RAT. Thus, Fig. 15 of Levy does not teach or suggest this limitation recited in claim 23."

Examiner disagrees. Applicant states that "architectural registers in instructions are not logical registers." This is true; however, architectural registers are the same as physical registers. The architectural register of Levy is mapped to the physical register of the claim. The rename registers are equivalent to logical registers.

The argument that the RAT is not initialized is without merit. Col. 7 lines 47-58 indicate how the RAT works. In particular, the "valid bit" must be indicated with a zero when there is no entry. The table must be initialized accordingly for the RAT to know when a register is mapped appropriately.

5. Applicant states:

"Thus, Levy's embodiment 1 does not have a freelist of registers and does not always divide registers in half because if there are 3 threads, all registers will be partitioned into 3 sets. Therefore, Levy's embodiment 1 does not teach or suggest this limitation recited in claim 23."

Examiner disagrees. Applicant appears to be under the misconception that if an embodiment exists within the reference that does not address all limitations of a claim, then the reference itself does not address all limitations of the claim. This is simply not true. Applicant points out that if there are 3 threads in Levy, then the registers are partitioned in 3 ways, and, therefore, cannot be divided in "half". While this is true, this does not address the clear fact that the invention was created to utilize only two threads as well; these two threads result in a 2-way division of the registers and Applicant's claimed limitations are met by this disclosure.

Perhaps Applicant is arguing that Levy never discloses using precisely two threads. If this is the case, the argument is without merit. The graphs on Figs. 6-8 disclose the use of two threads.

6. Applicant states:

"Applicants cannot find from the cited portion of Leibholz anything, expressly or inherently, that physical registers in a physical register file are to be divided equally among a plurality of threads when operating in MT mode, as recited in claim 1."

Examiner apologizes of the explanation of the combination was in some way unclear. The first citation (col. 1 lines 56-67) indicates that "[i]n multithreaded mode, each active thread may have an associated register file which the thread may access." To clarify, col 4 lines 5-7 states, "with multi-thread mode, each thread has access to only a single one of the register files 20A and 20B." Therefore, we know that the registers of 20A and 20B are divided among the threads. The only remaining requirement is that register files 20A and 20B are equal in size.

Applicant's attention is addressed to the second citation (col. 4 lines 19-20) states that "The registers 20A and 20B hold identical contests." For this to be true, they must be the same size. Accordingly, they appear to be the same size in fig. 2A and 2B.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the

objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100